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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,615	01/27/2004	Shiv Kumar Gupta	15397US01	1349

23446 7590 03/27/2008

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EXAMINER	
MANOSKEY, JOSEPH D	
ART UNIT	PAPER NUMBER
2113	

MAIL DATE	DELIVERY MODE
03/27/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/765,615	GUPTA ET AL.	
	Examiner	Art Unit	
	JOSEPH D. MANOSKEY	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☒ Claim(s) *15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 15 is objected to because of the following informalities: Claim 15 cites both inputs of the multiplexer being the first selection. The Examiner believes this to be a typographical error and the second "the first selection" should read "the second selection. It will be interpreted a such for the purposes of further examination. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rana, U.S. Patent 5,968,188, in view of Agarwal, U.S. Patent App. Pub. 2001/0013119.

4. Referring to claim 1, Rana teaches a emulation circuit, which provides real-time code coverage data, connected to a target system via an address line, a data line, and a control line of a ROM socket, this is interpreted as a circuit for analyzing code coverage of firmware by test inputs, said circuit comprising: an input for receiving an

address from a code address bus (See Fig. 2, Col. 1, lines 5-10, and Col. 7, lines, lines 49-51). Rana discloses a code coverage memory comprised of multiple locations and the code coverage memory being concurrently addressed with the monitored memory, this is interpreted as a memory for storing recorded addresses form the code address bus, the memory comprising a plurality of memory locations, each of the memory locations mapped to a particular one of a corresponding plurality of addresses associated with the firmware (See Fig. 2, Col. 2, line 55 to Col. 3, line 10 and Col. 5, lines 11-18).

Rana does not teach the contents of the memory location associated with the address received from the code address bus being incremented responsive to the receipt of the address, however Rana does teach the code coverage memory storing code coverage data of predetermined bit patterns that includes hexadecimal value "00" and changed to value "ff" to determine if the code has been executed (See Col. 8, lines 31-44). Agarwal discloses code coverage testing and flagging code that has been executed. In addition to just flagging the code that has been executed, Agarwal also teaches incrementing a value of the associated memory (See Agarwal, paragraphs 0123, 0124, and 0127). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the use of a predetermined bit pattern of the executed code of Rana with the storing of an incremented value associated with executed code of Agarwal. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because it allows for keeping count of the number of times the code has been executed (See Agarwal, paragraph 0124).

5. Referring to claim 2, Rana and Agarwal disclose all the limitations (See rejection of claim 1) including the code coverage memory being concurrently addressed with the monitored memory and the use of a counter circuit of memory location, where the cover memory can be isolated from the addressing from the monitored memory, thus selecting counter circuit and the address lines being multiplexed, this is interpreted as an address multiplexer for making a selection between the input and an address counter, and for providing the selection to the memory (See Rana, Col. 4, line 65 to Col. 5, line 3, Col. 5, lines 11-18, and Col. 10, lines 63-64).

6. Referring to claim 3, Rana and Agarwal teach all the limitations (See rejection of claim 1) including Rana teaches the code coverage memory storing code coverage data of predetermined bit patterns that includes setting the hexadecimal value to “00” and changing it to value “ff” and the data lines being multiplexed. Agarwal teaches the values for a test run being ‘1’ for set, thus ‘0’ being the cleared value and incrementing the value, this is interpreted as a data multiplexer for making a selection between an increment signal and a clear signal, and for providing the selection to the memory (See Rana Col. 8, lines 31-44, Col. 10, lines 63-64 and See Agarwal, paragraphs 0123 and 0124).

7. Referring to claim 4, Rana and Agarwal teach all the limitations (See rejection of claim 3) including the code coverage memory storing code coverage data of

predetermined bit patterns that includes setting the hexadecimal value to "00" and changing it to value "ff" to locations accessed for each test, this is interpreted as wherein if the data multiplexer selects the clear signal, and if the address multiplexer selects the address counter, then a memory location mapped to an address from the address counter is cleared (See Rana, Col. 8, lines 31-44).

8. Referring to claim 5, Rana teaches a method of real-time code coverage with a emulation circuit connected to a target system via an address line, a data line, and a control line of a ROM socket, this is interpreted as a method for analyzing code coverage, said method comprising: receiving an address form a code address bus, the address associated with an instruction in a system on a chip (See Fig. 2, Col. 1, lines 5-10, and Col. 7, lines, lines 49-51). Rana discloses a code coverage memory comprised of multiple locations and the code coverage memory being concurrently addressed with the monitored memory (See Fig. 2, Col. 2, line 55 to Col. 3, line 10 and Col. 5, lines 11-18).

Rana does not teach incrementing a memory location mapped to the address associated with the instruction, however Rana does teach the code coverage memory storing code coverage data of predetermined bit patterns that includes hexadecimal value "00" and changed to value "ff" (See Col. 8, lines 31-44). Agarwal discloses code coverage testing and flagging code that has been executed. In addition to just flagging the code that has been executed, Agarwal also teaches incrementing a value of the associated memory (See Agarwal, paragraphs 0123, 0124, and 0127). It would have

been obvious to one of ordinary skill in the art at the time of the invention to combine the use of a predetermined bit pattern of the executed code of Rana with the storing of an incremented value associated with executed code of Agarwal. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because it allows for keeping count of the number of times the code has been executed (See Agarwal, paragraph 0124).

9. Referring to claim 6, Rana and Agarwal disclose all the limitations (See rejection of claim 5) including the code coverage memory being concurrently addressed with the monitored memory and the use of a counter circuit of memory location and the address lines being multiplexed, this is interpreted as selecting between the input and an address counter; and providing the selection to the memory (See Rana, Col. 4, line 65 to Col. 5, line 3, Col. 5, lines 11-18, and Col. 10, lines 63-64).

10. Referring to claim 7, Rana and Agarwal teach all the limitations (See rejection of claim 5) including Rana teaches the code coverage memory storing code coverage data of predetermined bit patterns that includes setting the hexadecimal value to “00” and changing it to value “ff” and the data lines being multiplexed. Agarwal teaches the values for a test run being ‘1’ for set, thus ‘0’ being the cleared value and incrementing the value, this is interpreted as selecting between an increment signal and a clear signal; and providing the selection to the memory (See Rana, Col. 8, lines 31-44 Col. 10, lines 63-64, Agarwal, paragraphs 0123 and 0124).

11. Referring to claim 8, Rana and Agarwal teach all the limitations (See rejection of claim 7) including the code coverage memory storing code coverage data of predetermined bit patterns that includes setting the hexadecimal value to "00" and changing it to value "ff" to locations accessed for each test, this is interpreted as wherein if the clear signal is selected, and if the address counter is selected, then clearing a memory location mapped to an address from the address counter (See Agarwal, Col. 8, lines 31-44).

12. Referring to claim 9, Rana teaches a emulation circuit, which provides real-time code coverage data, connected to a target system via an address line, a data line, and a control line of a ROM socket, this is interpreted as a circuit for analyzing code coverage of firmware by test inputs, said circuit comprising: an input for receiving an address from a code address bus (See Fig. 2, Col. 1, lines 5-10, and Col. 7, lines, lines 49-51). Rana discloses a code coverage memory comprised of multiple locations and the code coverage memory being concurrently addressed with the monitored memory, this is interpreted as a memory operably connected to the input for storing recorded addresses form the code address bus, the memory comprising a plurality of memory locations, each of the memory locations mapped to a particular one of a corresponding plurality of addresses associated with the firmware (See Fig. 2, Col. 2, line 55 to Col. 3, line 10 and Col. 5, lines 11-18).

Rana does not teach the contents of the memory location associated with the address received from the code address bus being incremented responsive to the receipt of the address, however Rana does teach the code coverage memory storing code coverage data of predetermined bit patterns that includes hexadecimal value "00" and changed to value "ff" (See Col. 8, lines 31-44). Agarwal discloses code coverage testing and flagging code that has been executed. In addition to just flagging the code that has been executed, Agarwal also teaches incrementing a value of the associated memory (See Agarwal, paragraphs 0123, 0124, and 0127). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the use of a predetermined bit pattern of the executed code of Rana with the storing of an incremented value associated with executed code of Agarwal. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because it allows for keeping count of the number of times the code has been executed (See Agarwal, paragraph 0124).

13. Referring to claim 10, Rana and Agarwal disclose all the limitations (See rejection of claim 9) including the code coverage memory being concurrently addressed with the monitored memory and the use of a counter circuit of memory location, where the cover memory is isolated from the addressing from the monitored memory, thus selecting counter circuit and the address lines being multiplexed, this is interpreted as an address multiplexer connected to the input and address counter, the address multiplexer making a selection between the input and an address counter, and for

providing the selection to the memory (See Rana, Col. 4, line 65 to Col. 5, line 3, Col. 5, lines 11-18, and Col. 10, lines 63-64).

14. Referring to claim 11, Rana and Agarwal teach all the limitations (See rejection of claim 9) including Rana teaching the code coverage memory storing code coverage data of predetermined bit patterns that includes setting the hexadecimal value to "00" and changing it to value "ff" and the data lines being multiplexed. Agarwal teaches the values for a test run being '1' for set, thus '0' being the cleared value and incrementing the value, this is interpreted as a data multiplexer connected to the memory, the data multiplexer selecting between an increment signal and a clear signal, and providing the selection to the memory (See Rana, Col. 8, lines 31-44, Col. 10, lines 63-64 and See Agarwal, paragraphs 0123 and 0124).

15. Referring to claim 12, Rana and Agarwal teach all the limitations (See rejection of claim 11) including the code coverage memory storing code coverage data of predetermined bit patterns that includes setting the hexadecimal value to "00" and changing it to value "ff" to locations accessed for each test, this is interpreted as wherein if the data multiplexer selects the clear signal, and if the address multiplexer selects the address counter, then a memory location mapped to an address from the address counter is cleared (See Rana, Col. 8, lines 31-44).

16. Referring to claim 13, Rana and Agarwal teach all the limitations (See rejection of claim 1) including incrementing the value of the associated value of memory, thereby keeping a count of the number of times the code has executed, this is interpreted as wherein the contents of the memory location associated with the address received from the code address bus are incremented responsive to receipt of the address, thereby indicating a number of times the addressed has been received (See Agarwal, paragraph 0124).

17. Referring to claim 14, Rana and Agarwal disclose all the limitations (See rejection of claim 2) including the code coverage memory being concurrently addressed with the monitored memory and the use of a counter circuit of memory location, where the cover memory can be isolated from the addressing from the monitored memory, thus selecting counter circuit and the address lines being multiplexed. Rana also teaches the address lines being multiplexed. This is interpreted as wherein the multiplexer further comprises a first input that is directly connected to the input for receiving an address from a code address bus; a second input that is directly connected to the address counter; and an output that is directly connected to the memory. (See Rana, Col. 4, line 65 to Col. 5, line 3, Col. 5, lines 11-18, and Col. 10, lines 63-64).

18. Referring to claim 15, Rana and Agarwal disclose all the limitations (See rejection of claim 14) including isolating to the code coverage memory or not, this is interpreted as wherein multiplexer directly connects the first input to the output if the

input for receiving an address from a code address bus is the first selection and directly connects the second input to the output if the address counter is the first selection (See Rana, Col. 4, line 63 to Col. 5, line 3).

19. Referring to claim 16, Rana and Agarwal disclose all the limitations (See rejection of claim 15) including isolating to the code coverage memory or not, this is interpreted as wherein the first selection is sometimes the input for receiving an address from a code address bus and is sometimes the address counter (See Rana, Col. 4, line 63 to Col. 5, line 3).

Response to Arguments

20. Applicant's arguments filed pages 1-3 of remarks filed 14 February 2008, regarding claim 1 have been fully considered but they are not persuasive. The Applicant argues that Rana and Agarwal are not combinable because the use of the incremental value of Agarwal would overwrite the predetermined bit pattern of Rana and render Rana unsatisfactory for its intended purpose. The Examiner respectfully disagrees. Rana uses one known value to indicate code that has not been executed and one known value to indicate code that has been executed. Agarwal allows for indicating that code has been executed and also how many times it has been executed. The use of the incremented value does not render the predetermined value unsatisfactory for its purpose, but rather enhances it. Therefore a first “predetermined” value is used to indicate the code has not been executed and additional “predetermined” values are

used to indicate the code has been executed along with additional information indicating the number times it has been executed.

Referring to claims 2 and 10, the Applicant argue that the prior art does not teach "an address multiplexer for making a first selection between the input and an address counter, and for providing the first selection to memory. The Examiner respectfully disagrees. Rana teaches the address lines of the emulation circuit being multiplexed (See Rana, Col. 10, lines 63-64).

Conclusion

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOSEPH D. MANOSKEY whose telephone number is (571)272-3648. The examiner can normally be reached on Mon.-Fri. (7:30am to 4pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JDM
March 21, 2008

/Robert W. Beausoliel, Jr./
Supervisory Patent Examiner, Art Unit 2113